Benchmarking Round 2 Candidates on Microcontrollers

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Motivation and Scope

• Motivation
  • Evaluate the performance of Round 2 candidates on microcontrollers
  • Compare the candidates against existing NIST standards

• Goals
  • High coverage of implementations
  • Wide range of test cases
  • Verification of the implementations and results

• Scope
  • API compatible implementations
  • Official versions of the algorithms
  • This presentation: only primary variants
Implementations

- Implementations were gathered from
  - Submission packages
  - Websites and GitHub repositories of the candidates
  - Third party software benchmarking projects

<table>
<thead>
<tr>
<th>Language*</th>
<th>AEAD (89 Variants)</th>
<th>Hash (19 Variants)</th>
<th>Total</th>
<th>AEAD-Primary (32 Variants)</th>
<th>Hash-Primary (12 Variants)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>161</td>
<td>41</td>
<td>202</td>
<td>66</td>
<td>27</td>
</tr>
<tr>
<td>C / AVR</td>
<td>73</td>
<td>15</td>
<td>88</td>
<td>26</td>
<td>10</td>
</tr>
<tr>
<td>C / ARM / AVR</td>
<td>9</td>
<td>4</td>
<td>13</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>ARM</td>
<td>35</td>
<td>4</td>
<td>39</td>
<td>18</td>
<td>4</td>
</tr>
<tr>
<td>AVR</td>
<td>19</td>
<td>16</td>
<td>35</td>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>297</strong></td>
<td><strong>80</strong></td>
<td><strong>377</strong></td>
<td><strong>120</strong></td>
<td><strong>50</strong></td>
</tr>
</tbody>
</table>

*Languages used in a single implementation folder
Implentations - Remarks

• Primary variants of COMET*, ESTATE, mixFeed, and SAEAES* have only reference implementations.

• Problems faced in the benchmarking process
  • Build errors
  • Decryption failures
  • Program crash
  • Unsupported input sizes
  • Test vector verification failures

* Uses T-table based AES implementation.
# Platforms

<table>
<thead>
<tr>
<th>Board</th>
<th>Microcontroller / Core</th>
<th>Frequency</th>
<th>Flash</th>
<th>SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arduino Uno Rev3</td>
<td>ATmega328P - AVR (8-bit)</td>
<td>16 MHz</td>
<td>32 KB</td>
<td>2 KB</td>
</tr>
<tr>
<td>Arduino Nano Every</td>
<td>ATMega4809 - AVR (8-bit)</td>
<td>20 MHz</td>
<td>48 KB</td>
<td>6 KB</td>
</tr>
<tr>
<td>Arduino MKR Zero</td>
<td>SAMD21 - ARM Cortex-M0+ (32-bit)</td>
<td>48 MHz</td>
<td>256 KB</td>
<td>32 KB</td>
</tr>
<tr>
<td>Arduino Due</td>
<td>AT91SAM3X8E - ARM Cortex-M3 (32-bit)</td>
<td>84 MHz</td>
<td>512 KB</td>
<td>96 KB</td>
</tr>
<tr>
<td>Arduino Nano 33 BLE</td>
<td>nRF52840 - ARM Cortex-M4F (32-bit)</td>
<td>64 MHz</td>
<td>1 MB</td>
<td>256 KB</td>
</tr>
<tr>
<td>HiFive1 Rev B</td>
<td>SiFive FE310-G002 - RV32 IMAC (32-bit)</td>
<td>320 MHz</td>
<td>4 MB</td>
<td>16 KB</td>
</tr>
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Test Cases

• Time
  • Varying input sizes for *Plaintext* and *Associated Data* for AEAD and Hash functions
    • Short inputs: ranging from 0 to 128 bytes
    • Long inputs*: ranging from 256 to 2048 bytes with 128-byte increments

• Size
  • For AEAD algorithms, the sizes for *enc-only, dec-only* implementations are calculated.
  • Actual sizes are calculated by taking the difference w.r.t. the *empty cipher*.

*Omitted for AVR.*
The Benchmarking Framework

- The framework consists of C++ code for carrying out the experiments, and scripts for automating the build process and post-processing the results.
- It uses the PlatformIO embedded development platform and the GNU toolchains

1 (GNU Tools for Arm Embedded Processors 7-2017-q4-major) 7.2.1 20170904 (release) [ARM/embedded-7-branch revision 255204]
2 (GNU MCU Eclipse ARM Embedded GCC, 64-bit) 8.2.1 20181213 (release) [gcc-8-branch revision 267074]
3 (AVR_8_bit_GNU_Toolchain_3.6.2_1759) 5.4.0
### Build Configurations

#### Implementation

| AEAD-Impl₁ | 0 | 1 |
| AEAD-Impl₁₂₀ | 0 | 0 |

| Hash-Impl₁ | 0 | 1 |
| Hash-Impl₅₀ | 0 | 0 |

#### Mode

| LWC_MODE_GENKAT_AEAD | 0 |
| LWC_MODE_TIMING_AEAD | 1 |
| LWC_MODE_USE_AEAD_ENCRYPT | 0 |
| LWC_MODE_USE_AEAD_DECRYPT | 1 |
| LWC_MODE_USE_AEAD_BOTH | 0 |

| LWC_MODE_GENKAT_HASH | 0 |
| LWC_MODE_TIMING_HASH | 1 |
| LWC_MODE_USE_HASH | 0 |

#### Flags

- -Os
- -O1
- -O2
- -O3

#### Platform

- Arduino MKR Zero
- Arduino Uno
- Arduino Nano 33 BLE
• Code size (AEAD & Hash)
• Timing (AEAD & Hash)
• Pairwise-comparison of AEAD algorithms against AES-GCM (AEAD only)

• Benchmarks include AES-GCM and SHA-256 from Mbed-TLS library for comparison.
Code Size for Primary AEAD Variants* on Cortex-M0+

* Smallest sized implementation of each variant among all its implementations compiled with four different optimization flags
Code Size for Primary AEAD Variants* on Cortex-M4F

* Smallest sized implementation of each variant among all its implementations compiled with four different optimization flags
Code Size for Primary AEAD Variants* on AVR

* Smallest sized implementation of each variant among all its implementations compiled with four different optimization flags

[Bar chart showing the code size (bytes) for various AEAD variants on AVR.]
Timings for Primary AEAD Variants* on Cortex-M0+ (AD Length=0, Msg Length=16, 64, 2048)

* Fastest implementation of each variant among all its implementations compiled with four different optimization flags

The value over each bar is for Mlen = 2048
Timings for Primary AEAD Variants* on Cortex-M4F (AD Length=0, Msg Length=16, 64, 2048)

* Fastest implementation of each variant among all its implementations compiled with four different optimization flags

The value over each bar is for Mlen = 2048
Timings for Primary AEAD Variants* on AVR (AD Length=0, Msg Length=16, 32, 128)

* Fastest implementation of each variant among all its implementations compiled with four different optimization flags

The value over each bar is for $\text{Mlen} = 128$
Pairwise Comparison of AEAD Algorithms

- A 2D plot is created by comparing the execution times of two AEAD algorithms for each *Plaintext* and *Associated Data* length from 0 to 128 bytes.
Primary AEAD Variants¹ v. AES-GCM² on Cortex-M0+

<table>
<thead>
<tr>
<th>ACE</th>
<th>ASCON</th>
<th>COMET</th>
<th>DryGASCON</th>
<th>Elephant</th>
<th>ESTATE</th>
<th>ForkAE</th>
<th>GIFT-COFB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gimli</td>
<td>Grain-128AEAD</td>
<td>HyENA</td>
<td>ISAP</td>
<td>KNOT</td>
<td>LOTUS-LOCUS</td>
<td>mixFeed</td>
<td>ORANGE</td>
</tr>
<tr>
<td>Oribatida</td>
<td>PHOTON-Beetle</td>
<td>Pyjamask</td>
<td>Romulus</td>
<td>SAEAES</td>
<td>Saturnin</td>
<td>SKINNY-AEAD</td>
<td>SPARKLE</td>
</tr>
<tr>
<td>SPIX</td>
<td>SpoC</td>
<td>Spook</td>
<td>Subterranean 2.0</td>
<td>SUNDAE-GIFT</td>
<td>TinyJambu</td>
<td>WAGE</td>
<td>Xoodyak</td>
</tr>
</tbody>
</table>

¹ The fastest implementation of each variant. ² Mbed TLS implementation with `MBEDTLS_AES_ROM_TABLES` and `MBEDTLS_AES_FEWER_TABLES` defined.
<table>
<thead>
<tr>
<th>Primary AEAD Variants $^1$ v. AES-GCM $^2$ on Cortex-M4F</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ACE</strong></td>
</tr>
<tr>
<td>Gimli</td>
</tr>
<tr>
<td>Oribatida</td>
</tr>
<tr>
<td>SPIX</td>
</tr>
</tbody>
</table>

1 The fastest implementation of each variant. 2 Mbed TLS implementation with `MBEDTLS_AES_ROM_TABLES` and `MBEDTLS_AES_FEWER_TABLES` defined.
* Smallest sized implementation of each variant among all its implementations compiled with four different optimization flags.
Code Size for Primary Hash Variants* on Cortex-M4F

* Smallest sized implementation of each variant among all its implementations compiled with four different optimization flags.
Code Size for Primary Hash Variants* Variants on AVR

* Smallest sized implementation of each variant among all its implementations compiled with four different optimization flags.
Timings for Primary Hash Variants* on Cortex-M0+ (Msg Length=16, 64, 2048)

* Fastest implementation of each variant among all its implementations compiled with four different optimization flags

The value over each bar is for Mlen = 2048
Timings for Primary Hash Variants* on Cortex-M4F (Msg Length=16, 64, 2048)

* Fastest implementation of each variant among all its implementations compiled with four different optimization flags.

The value over each bar is for Mlen = 2048.
Benchmarking is challenging, due to the range of platforms, implementation tradeoffs, and different use cases.

**AEAD**

- Most of the candidates achieved smaller *code size* compared to AES-GCM*.
- On ARM Cortex-M0+ about half of the candidates and on ARM Cortex-M4F most candidates showed performance improvement at least in some of the test cases over AES-GCM*.

**Hash**

- Depending on the platform, four to seven candidates had smaller code size than SHA-256*.
- Most of the candidates performed worse compared to SHA-256 in timing experiments.

* Mbed TLS implementation.
• Fair and extensive performance evaluation of the candidates on microcontrollers will contribute to the selection of the finalists.

• The benchmark results published by the submitters, third party benchmarking projects, and academic papers are also taken into consideration in the evaluation process.

• The benchmarking framework and the results will be available at: https://github.com/usnistgov/Lightweight-Cryptography-Benchmarking

• Next Steps
  • Keep the implementation database up to date
  • Resolve the issues for implementations where benchmarking could not be performed
  • Add new platforms
  • Verify and publish the results
Contact

Project webpage: https://csrc.nist.gov/projects/lightweight-cryptography

GitHub: https://github.com/usnistgov/Lightweight-Cryptography-Benchmarking

Forum: lwc-forum@list.nist.gov

Contact email: lightweight-crypto@nist.gov