Public Use Document

Junos OS Physical Entropy Source – Intel Xeon D-2100 Series (Skylake) 18 Core Die with FCBGA2518 Package 1.0

TESTING
NVLAP LAB CODE 600247-0

Document Reference: ESV-E007 PUD 1.0
Document Status: Released
Client: Juniper Networks
Part I – Frontmatter and Clarifications: 6 pages excluding cover.
Part II – Vendor/Developer PUD: 15 pages including cover.

TERON LABS

Document Authorisation

Release Date:	28-Nov-2023
Version:	1.0
Document Identifier:	ESV-E007-PUD 1.0
Release Authority:	Yvonne Cliff

Copyright Notice

Teron Labs AISEF

Unit 3
10 Geils Court
Deakin, ACT 2600
Australia

+61 2 5114 4878
info@teronlabs.com
www.teronlabs.com

This report must not be used by the client to claim product certification approval or endorsement by NVLAP, the National Institute of Standards and Technology (NIST) or any other agency of the US Government.

Table of Contents

List of Tables

1 Document Management

Version	Date	Author	Description
1.0	28 Nov 2023	Yvonne Cliff	Initial Release

2 Introduction

2.1 Overview

This document is the Public Use Document for the NIST SP 800-90B Entropy Source Validation of Junos OS Physical Entropy Source – Intel Xeon D-2100 Series (Skylake) 18 Core Die with FCBGA2518 Package 1.0.

The document is in two parts. The second part is the Public Use Document as provided by the vendor/developer. The first part provides validation identifiers and any comments which Teron Labs provides in addition to the vendor/developer document.

2.2 Validation Identifiers

Document Title	Public Use Document for Junos OS Physical Entropy Source – Intel Xeon D-2100 Series (Skylake) 18 Core Die with FCBGA2518 Package
Document Identifier	ESV-E007-PUD 1.0
Document Version	1.0
IUT Name	Junos OS Physical Entropy Source – Intel Xeon D-2100 Series (Skylake) 18 Core Die with FCBGA2518 Package
IUT Version	1.0
Client	Juniper Networks 1133 Innovation Way Sunnyvale, CA, 94089, USA
Laboratory	Teron Labs Canberra Unit 3, 10 Geils Court, Deakin ACT 2600, Australia
Standards Applied	SP 800-90B for FIPS 140-3

Table 1 – Validation Identifiers

2.3 Standards Applied

Document	Title	Date
SP 800-90B	*Recommendation for Entropy Sources Used for Random Bit Generation*	Jan 2018

SP 800-90A	*Recommendation for Random Number Generation Using Deterministic Random Bit Generators*	June 2015
SP 800-90C	*Recommendation for Random Bit Generator (RBG) Constructions (2nd Public Draft)*	Apr 2016
Implementation Guidance	*Implementation Guidance for FIPS 140-3 and the Cryptographic Module Validation Program*	Aug 2023
90B Shall Statements	*Spreadsheet of SP 800-90B Shall Statements*	

Table 2 – Standards Applied

3 Evaluation Results

The laboratory concludes that the entropy source meets the SP 800-90B and related FIPS 140-3 IG requirements for entropy source validation and provides full entropy output.

Although the vendor/developer PUD Section 7 makes a claim of full entropy based on the use of the Output_Entropy function, the entropy source also outputs full entropy using the IG D.K definition.

However, to meet the IG D.K definition, the “Needed entropy rate” for the “XOR Feedback Decorrelator-Decimator” in Figure 7-1 of the vendor/developer PUD must be $192/512 = 0.375$ instead of 0.29. Similarly, the figure of 0.29 input entropy rate for the AES-CBC-MAC conditioner in the text below Figure 7-1 (Section 7, page 12) should also be revised to be 0.375 to meet the IG D.K definition of full entropy.

The NRBG construction/XOR (RBG3) construction is compliant with the SP 800-90C 2nd draft (April 2016), but not the SP 800-90C 3rd draft (September 2022) due to the security strength of the DRBG.

Intel Digital Random Number Generator SP800-90B Non-Proprietary Public Use Document

Intel Entropy Source

May 2023

Revision 0.3.4

Intel Confidential

Document Number: 715192

Notice: This document contains information on products in the design phase of development. The information here is subject to change without notice. Do not finalize a design with this information.

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software, or service activation. Learn more at intel.com, or from the OEM or retailer.

No computer system can be absolutely secure. Intel does not assume any liability for lost or stolen data or systems or any damages resulting from such losses.

You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document. The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

This document contains information on products, services and/or processes in development. All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest Intel product specifications and roadmaps.

Intel disclaims all express and implied warranties, including without limitation, the implied warranties of merchantability, fitness for a particular purpose, and non-infringement, as well as any warranty arising from course of performance, course of dealing, or usage in trade.

Tests document performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit http://www.intel.com/performance.

Cost reduction scenarios described are intended as examples of how a given Intel-based product, in the specified circumstances and configurations, may affect future costs and provide cost savings. Circumstances will vary. Intel does not guarantee any costs or cost reduction.

Results have been estimated or simulated using internal Intel analysis or architecture simulation or modeling and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance.

Intel does not control or audit third-party benchmark data or the web sites referenced in this document. You should visit the referenced web site and confirm whether referenced data are accurate.

Intel is a sponsor and member of the Benchmark XPRT Development Community and was the major developer of the XPRT family of benchmarks. Principled Technologies is the publisher of the XPRT family of benchmarks. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases.

Copies of documents which have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or by visiting www.intel.com/design/literature.htm.

Intel, the Intel logo, and Xeon are trademarks of Intel Corporation or its subsidiaries.

*Other names and brands may be claimed as the property of others

Contents

Figures

Tables

Revision History

Revision Number	Description	Date
0.3.4	• Initial release of the document.	May 2023

1 Description

The Intel Entropy Source is a Physical (P) entropy source.

The circuit component is RNG_ES_SKX_1.0

The synthesizable RTL component is SKX-COOP-RTL1.0

All components of the entropy source are hardware, consisting of logical and electronic components bounded in a rectangle of silicon. There is no firmware or software within the entropy source.

The entropic data from the entropy source is Non-Independent and Identically Distributed (IID).

This PUD is applicable to the following products:

Table 1-1. List of Applicable Devices

Processor Name	Processor Name
Intel® Xeon® D-2123IT Processor	Intel® Xeon® D-2166NT Processor
Intel® Xeon® D-2141I Processor	Intel® Xeon® D-2168NT Processor
Intel® Xeon® D-2142IT Processor	Intel® Xeon® D-2173IT Processor
Intel® Xeon® D-2143IT Processor	Intel® Xeon® D-2177NT Processor
Intel® Xeon® D-2145NT Processor	Intel® Xeon® D-2178NT Processor
Intel® Xeon® D-2146NT Processor	Intel® Xeon® D-2183IT Processor
Intel® Xeon® D-2148NT Processor	Intel® Xeon® D-2187NT Processor
Intel® Xeon® D-2161I Processor	Intel® Xeon® D-2191 Processor
Intel® Xeon® D-2163IT Processor	Intel® Xeon® D-2191A Processor
Intel® Xeon® D-2164IT Processor	

2 Security Boundary

The entropy source security boundary surrounds the set of components referred to as the Digital Random Number Generator (DRNG) core that includes the noise source digitizer, Continuous Health Tests (CHT), Advanced Encryption Standard (AES)- Cipher Block Chaining - Message Authentication Code (CBC-MAC) Vetted Conditioning Component, Digital Random Number Generator (DRNG), Non-Deterministic Random Bit Generator (NRBG), and register interface.

For use as a full entropy source, the NRBG output of the DRNG is the necessary output. This is accessed through the Intel CPU instruction "RdSeed".

The security boundary is a sub boundary within the DRNG. Components outside the security boundary but within the DRNG are to attach to the local bus, clock, and power systems on the chip.

The DRNG security boundary is not a FIPS140 security boundary. It is designed to be usable within a larger FIPS140 security boundary through compliance with SP800-90A, B and draft C along with relevant requirements in ISO/IEC 19790-2012 and FIPS140-3.

The bold outline in Figure 2-1 shows the security boundary of the entropy source and other RNG components.

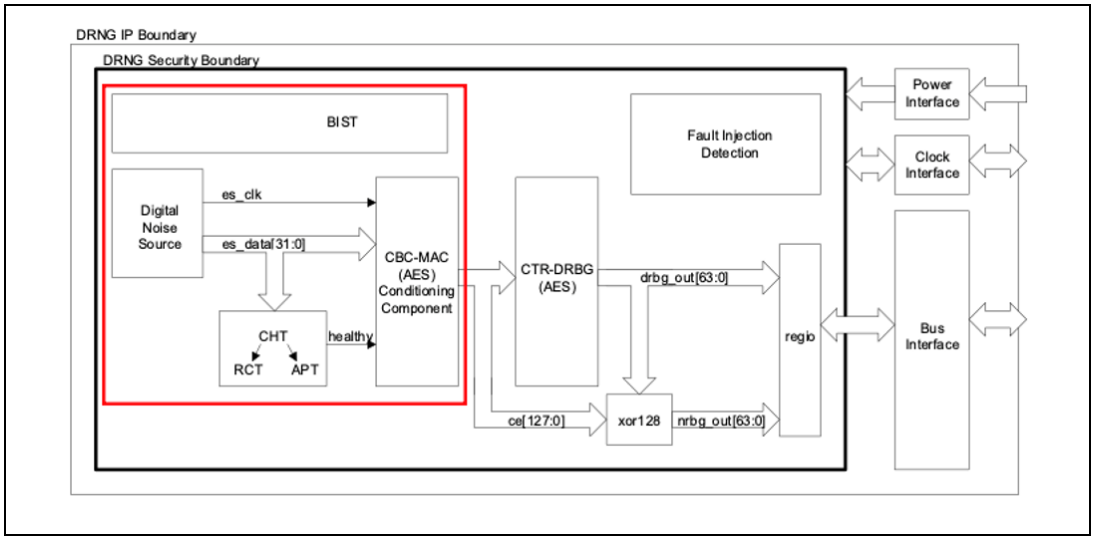
The NRBG output path to the region block is the output of the full entropy source, as an RBG3 construction.

The DRBG output path to the region block is the output of the DRBG, as an RBG2 construction.

The NRBG construction is the XOR (RBG3) construction NRBG from Draft SP800-90C. This XORs the output of the conditioner with an output from the DRBG to form the NRBG output. The strength of the XOR is entirely dependent on the full entropy of the conditioner output. The DRBG's input into the XOR, as well as the XOR operation itself are not considered part of the conditioning chain.

The width of these operations is 128 bits, driven by the output size of AES. The registers sizes are 64 bits and in the logic, this width transforming is performed using a FIFO that is 64 bits wide and takes in 128 bits as two 64-bit entries and outputs 64 bits to match the register width.

Figure 2-1. DRBG Security Boundary



In the context of an Intel CPU, the DRNG register that presents the NRBG output to the local bus is called `egetdata`. This register is read by the CPU whenever the `RdSeed` instruction is executed. The result is passed to the target register of the instruction and the success or failure signaled in the carry flag.

This report is applicable to the devices in Table 1-1. The silicon manufacturing process, IC design and DRNG design are identical for each of these devices. Differences between these devices are the set of enabled features, which has no influence on the RNG behavior.

3 Operating Conditions

The entropy source is guaranteed to operate within the designated operating envelope in the datasheet of the chip. In **Intel® Xeon® D-2191 Processor the** operating envelope is as follows:

Table 3-1. Operating Conditions

Parameter	Minimum	Maximum
Temperature	0 °C	80 °C

These conditions are taken from the Intel Automated Relational Knowledge-Base (ARK) specifications: https://www.intel.com/content/www/us/en/products/sku/129488/intel-xeon-d2191-processor-24-75m-cache-1-60-ghz/specifications.html

4 Configuration Settings

There are no configuration settings accessible at any privilege level to software running in the CPU.

5 Physical Security Mechanisms

The RNG contains a security boundary described in Section 2. In the operating mode of the RNG, there is hardware enforcement of the security of the boundary.

Specifically:

- Diagnostic output of raw data from the boundary is disabled.
- Debugging port access to internal state of the RNG is disabled at the boundary.
- Configuration input written to registers is ignored and the default configuration is enforced.
- Algorithms are implemented to detect stuck output failures.
- Register write privileges are enforced in hardware.

When an alarm is triggered, the RNG resets itself and re-runs Built-In Self-Test (BIST). It is not possible to distinguish between a failure due to attack or environmental bounds violation or a rare false positive error. The re-running of BIST will lead to the RNG failing if the BIST fails. In the case of a transitory error, the RNG will recover when BIST is re-run.

The packaging of the chip is a tamper evident enclosure.

6 Conceptual Interfaces

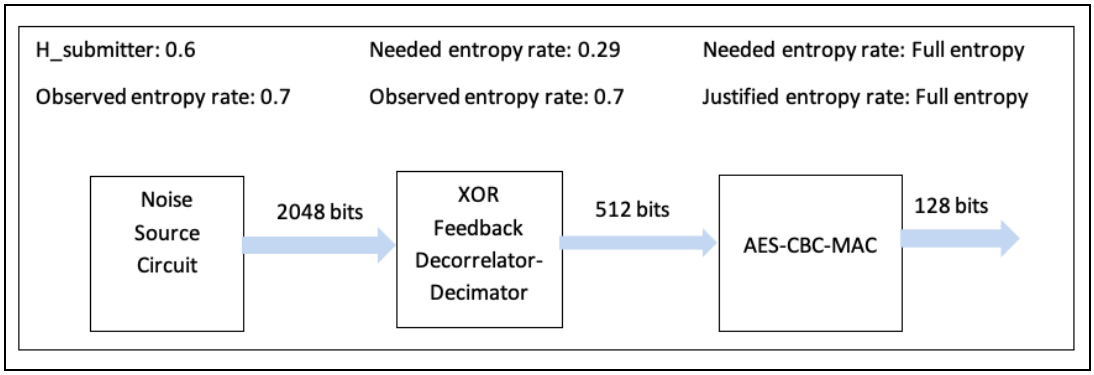
For consuming applications running in software on the CPU, `GetEntropy(n)` is implemented by the `RdSeed` instruction, where *n* can be one of 16, 32 or 64, depending on the size of the target register.

Internally to the security boundary, for feeding conditioner output data to the DRBG, `Get_entropy()` is implemented in digital logic between the conditioner and DRBG in the form of a 128-bit wide FIFO.

7 Minimum Entropy Rate

Figure 7-1 illustrates the required min-entropy rate and the actual observed min-entropy rate of the noise source and the chain of conditioners consisting of a non-vetted XOR Feedback Decorrelator-Decimator and a vetted AES-CBC-MAC. The XOR Feedback Decorrelator-Decimator is a digitizer per design, but for the sake of 90B compliance, it is treated as a non-vetted conditioner.

Figure 7-1. Entropy Levels on Noise Source and Conditioning Chain



The output of the AES-CBC-MAC conditioner has the full entropy, given that the input to the AES-CBC-MAC has an entropy rate that is greater than 0.29. The ≥0.29 entropy rate requirement from the digitized noise source is based on the SP 800-90B section 3.1.5.1.1 equation for the minimum input entropy requirement of the vetted AES-CBC-MAC conditioner.

The 0.6 entropy rate on the pre-digitizer data is a design target across all variants of silicon. The actual observed entropy rate on the noise source prior to digitization on the Intel CPU is greater than 70%. The digitization stage does not reduce the entropy rate, and it is observed that the entropy rate of the post-digitizer data feeding into the AES-CBC-MAC conditioner is greater than 0.7. The difference between the 0.29 and 0.7 entropy rates is the engineering margin in the design of the entropy source.

8 Health Tests

The DRNG includes:

- Continuous Health Tests (CHT).
- Startup Noise Source Health Tests.
- Startup Logic Integrity BIST.

The CHT is composed of a short-term test yielding a pass/fail over individual 256-bit blocks of noise source data, and a long-term evaluation of the pass/fail history of the past 256 blocks (totaling 65536 bits) to infer an entropy source failure. The failure condition is invoked when the pass/fail rate drops below 50%.

The logic integrity test is one of the startup tests. This performs a test of the digital logic by running deterministic random sequences through all the logic and testing the resulting output against the expected result.

The Startup Noise Source Health Test involves running the CHT for a probationary period of 65536 bits from the noise source. When the test is complete, assuming the test passes, the RNG enters the operational state. This happens during CPU startup and completes before the first CPU instructions can execute. Thus, `RdSeed` is available from initial instruction execution time.

The startup test is invoked at power-on or exiting the reset state. Thus, the startup tests can be invoked by power cycling the CPU or resetting the CPU.

A failure any of the startup tests (logic integrity or noise source health test) will be reflected as a BIST failure in the internal status register, which leads to an MCHECK failure of the CPU.

Following the startup tests, the CHT continues to run. Should failure condition of the CHT test be encountered after the startup tests have completes, this may be either the result of a soft error or a hard error. The test will continue to run and should the entropy quality return, it will exit the failure state. In the failure state, no more random numbers are issued, and the failure state is reflected in the internal state registers, which is visible at the instruction interface by the repeated failure to deliver random numbers, through the returned carry flag of the `RdRand` and `RdSeed` instructions being 0.

A sequence of 1000 back-to-back 0 carry flags on `RdSeed` can be inferred to be an error. Should some condition exist (for example, out of specification operating condition), cessation of that condition will lead to resumption of the supply of random numbers.

A less computationally expensive test of failure is the response from the `RdRand` instruction (not a noise source output, but an RBG2 output), which due to its higher output rate has a 0% chance of underflows arising from high consumption demand by other threads, and so 10 back-to-back failures are specified as a runtime error.

9 Maintenance

There are no maintenance action requirements.

10 Required Testing

We performed raw noise testing using the non-IID lower bound entropy tests of the SP800-90B Entropy Assessment software tool, showing the entropy from the noise source to exceed the minimum input threshold of 0.299 of the vetted conditioning components.

We performed restart testing using the SP800-90B Entropy Assessment software tool, showing the startup min entropy of *Hr* and *Hc* to be greater than 50% of *HI*.