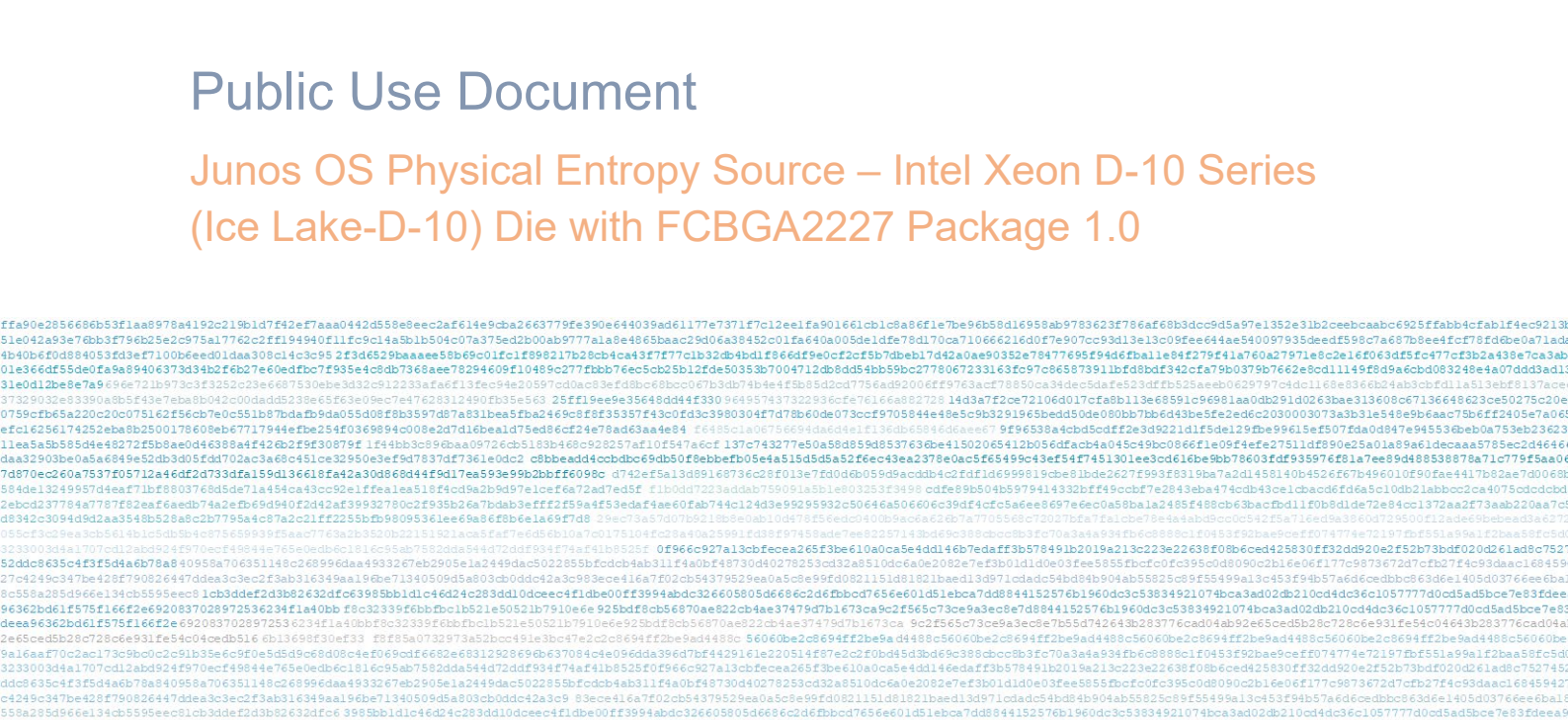
Public Use Document

Junos OS Physical Entropy Source – Intel Xeon D-10 Series (Ice Lake-D-10) Die with FCBGA2227 Package 1.0



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Teron Labs AISEF

Unit 3
10 Geils Court
Deakin, ACT 2600
Australia

+61 2 5114 4878
info@teronlabs.com
www.teronlabs.com

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1 Document Management

Version	Date	Author	Description
1.0	20-Feb-2024	Yvonne Cliff	Initial Release
1.1	24-May-2024	Yvonne Cliff	Inserted §3.1 (Disclaimers). Vendor/developer PUD updated to Revision 0.5, May 2024 (changes to §10, Required Testing).

2 Introduction

2.1 Overview

This document is the Public Use Document for the NIST SP 800-90B Entropy Source Validation of Junos OS Physical Entropy Source – Intel Xeon D-10 Series (Ice Lake-D-10) Die with FCBGA2227 Package 1.0.

The document is in two parts. The second part is the Public Use Document as provided by the vendor/developer. The first part provides validation identifiers and any comments which Teron Labs provides in addition to the vendor/developer document.

2.2 Validation Identifiers

Document Title	Public Use Document for Junos OS Physical Entropy Source – Intel Xeon D-10 Series (Ice Lake-D-10) Die with FCBGA2227 Package
Document Identifier	ESV-E008-PUD 1.1
Document Version	1.1
IUT Name	Junos OS Physical Entropy Source – Intel Xeon D-10 Series (Ice Lake-D-10) Die with FCBGA2227 Package
IUT Version	1.0
Client	Juniper Networks 1133 Innovation Way Sunnyvale, CA, 94089, USA
Laboratory	Teron Labs Unit 3, 10 Geils Court, Deakin ACT 2600, Australia

Table 1 – Validation Identifiers

2.3 Standards Applied

Document	Title	Date
SP 800-90B	*Recommendation for Entropy Sources Used for Random Bit Generation*	Jan 2018
SP 800-90A	*Recommendation for Random Number Generation Using Deterministic Random Bit Generators*	June 2015
SP 800-90C	*Recommendation for Random Bit Generator (RBG) Constructions (2nd Public Draft)*	Apr 2016
Implementation Guidance	*Implementation Guidance for FIPS 140-3 and the Cryptographic Module Validation Program*	Jan 2024
90B Shall Statements	*Spreadsheet of SP 800-90B Shall Statements*	

Table 2 – Standards Applied

3 Evaluation Results

3.1 Disclaimers

All data was collected by the vendor/developer. Results apply to the data samples as received.

Information about the entropy source was provided by the vendor/developer. The validity of the laboratory's findings is dependent on this information being accurate.

The findings of this evaluation are specific to the particular part/version, operational environment and entropy-relevant parameters that are documented and do not apply more broadly. If the entropy-relevant parameters are different than those described in this document, then additional modelling and statistical testing are required. Any part/version or configuration other than that described is not covered by this document.

3.2 Results

The laboratory concludes that the entropy source meets the SP 800-90B and related FIPS 140-3 IG requirements for entropy source validation and provides full entropy output.

Although the vendor/developer PUD Section 7 makes a claim of full entropy based on the use of the Output_Entropy function, the entropy source also outputs full entropy using the IG D.K definition.

However, to meet the IG D.K definition, the "Needed entropy rate" for the "XOR Feedback Decorrelator-Decimator" in Figure 7-1 of the vendor/developer PUD must be $192/512 = 0.375$ instead of 0.29. Similarly, the figure of 0.29 input entropy rate for the AES-CBC-MAC conditioner in the text below Figure 7-1 (Section 7, page 12) should also be revised to be 0.375 to meet the IG D.K definition of full entropy.

The NRBG construction/XOR (RBG3) construction is compliant with the SP 800-90C 2nd draft (April 2016), but not the SP 800-90C 3rd draft (September 2022) due to the security strength of the DRBG.



Intel's Digital Random Number Generator (DNGR) SP800-90B Non-Proprietary Public Use Document

Intel Entropy Source

May 2024

Revision 0.5

Intel Confidential

Document Number: 786463



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Revision History

Revision Number	Description	Date
0.5	• Chapter 10 updated.	May 2024
0.3.4	• Initial release	September 2023

1 Description

The Intel's Digital Random Number Generator (DNGR) Entropy Source is a Physical (P) entropy source.

The circuit component is RNG_ES_ICX_1.0

The synthesizable RTL component is ICX-COOP-RTL1.0

All components of the entropy source are hardware, consisting of logical and electronic components bounded in a rectangle of silicon. There is no firmware or software within the entropy source.

The entropic data from the entropy source is Non-IID.

This PUD is applicable to the following products:

Table 1-1. List of Applicable Devices

Processor Name	Processor Name
Intel® Xeon® D-1702 Processor	Intel® Xeon® D-1733NT Processor
Intel® Xeon® D-1702 Processor	Intel® Xeon® D-1734NT Processor
Intel® Xeon® D-1712TR Processor	Intel® Xeon® D-1735TR Processor
Intel® Xeon® D-1713NT Processor	Intel® Xeon® D-1736 Processor
Intel® Xeon® D-1713NTE Processor	Intel® Xeon® D-1736NT Processor
Intel® Xeon® D-1714 Processor	Intel® Xeon® D-1739 Processor
Intel® Xeon® D-1715TER Processor	Intel® Xeon® D-1746TER Processor
Intel® Xeon® D-1718T Processor	Intel® Xeon® D-1747NTE Processor
Intel® Xeon® D-1722NE Processor	Intel® Xeon® D-1748TE Processor
Intel® Xeon® D-1726 Processor	Intel® Xeon® D-1749NT Processor
Intel® Xeon® D-1732TE Processor	

2 Security Boundary

The DRNG security boundary surrounds the set of components referred to as the DRNG core, that includes the noise source, digitizer, Continuous Health Tests (CHT), AES-CBC-MAC Vetted Conditioning Component, DRBG, NRBG and register interface.

For use as a full entropy source, the NRBG output of the DRNG is the necessary output. This is accessed through the Intel CPU instruction “RdSeed”.

The security boundary is a sub boundary within the DRNG. Components outside the security boundary but within the DRNG are to attach to the local bus, clock and power systems on the chip.

The DRNG security boundary is not a FIPS140 security boundary. It is designed to be usable within a larger FIPS140 security boundary through compliance to SP800-90Arev1, B and draft C along with relevant requirements in ISO/IEC 19790-2012 and FIPS140-3.

The bold outline in Figure 2-1 shows the security boundary of the entropy source and other RNG components.

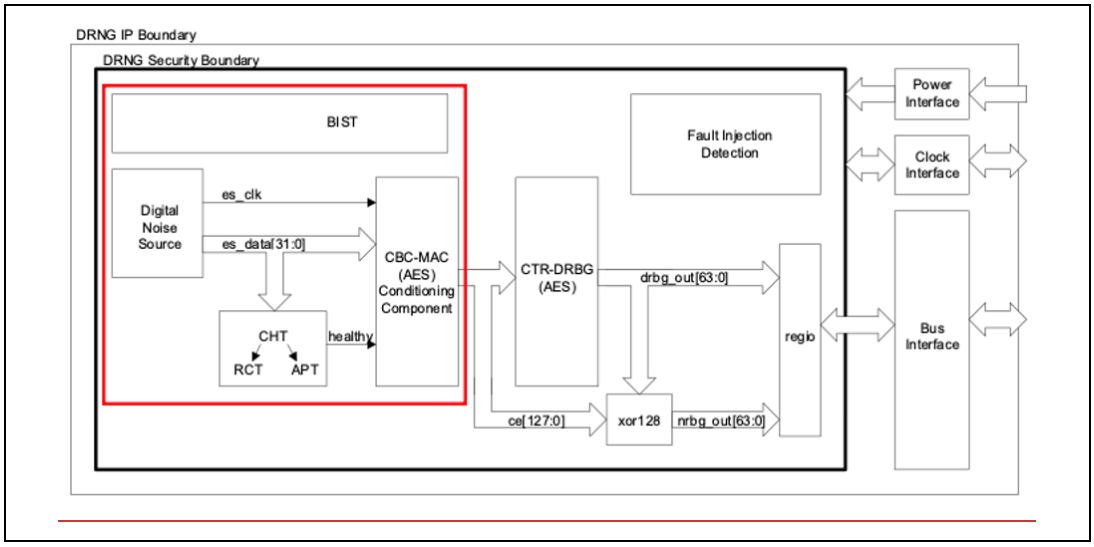
The NRBG output path to the region block is the output of the full entropy source, as an RBG3 construction.

The DRBG output path to the region block is the output of the DRBG, as an RBG2 construction.

The NRBG construction is the XOR (RBG3) construction NRBG from Draft SP800-90C. This XORs the output of the conditioner with an output from the DRBG to form the NRBG output. The strength of the XOR is entirely dependent on the full entropy of the conditioner output. The DRBG’s input into the XOR, as well as the XOR operation itself are not considered part of the conditioning chain.

The width of these operations is 128 bits, driven by the output size of AES. The registers sizes are 64 bits and in the logic, this width transforming is performed using a FIFO that is 64 bits wide and takes in 128 bits as two 64-bit entries and outputs 64 bits to match the register width.

Figure 2-1. DRBG Security Boundary



In the context of an Intel CPU, the DRNG register that presents the NRBG output to the local bus is called `egetdata`. This register is read by the CPU whenever the `RdSeed` instruction is executed. The result is passed to the target register of the instruction and the success or failure signaled in the carry flag.

This report is applicable to the devices in Table 1-1. The silicon manufacturing process, IC design and DRNG design is identical for each of these devices. Differences between these devices are the set of enabled features, which has no influence on the RNG behavior.

3 Operating Conditions

The entropy source is guaranteed to operate within the designated operating envelope in the data sheet of the chip. In **Intel® Xeon® D-1747NTE Processor** the operating envelope is as follows:

Table 3-1. Operating Conditions

Parameter	Minimum	Maximum
Temperature	0°C	77°C

These conditions are taken from the Intel ARK specifications:

https://www.intel.com/content/www/us/en/products/sku/226116/intel-xeon-d1747nte-processor-15m-cache-up-to-3-50-ghz/specifications.html

4 Configuration Settings

There are no configuration settings accessible at any privilege level to software running in the CPU.

5 Physical Security Mechanisms

The RNG contains a security boundary described in Section 2. In the operating mode of the RNG, there is hardware enforcement of the security of the boundary.

Specifically:

- Diagnostic output of raw data from the boundary is disabled.
- Debugging port access to internal state of the RNG is disabled at the boundary.
- Configuration input written to registers is ignored and the default configuration is enforced.
- Algorithms are implemented to detect stuck output failures.
- Register write privileges are enforced in hardware.

When an alarm is triggered, the RNG resets itself and re-runs BIST. It is not possible to distinguish between a failure due to attack or environmental bounds violation or a rare false positive error. The re-running of BIST will lead to the RNG failing if the BIST fails. In the case of a transitory error, the RNG will recover when BIST is re-run.

The packaging of the chip is a tamper evident enclosure.

6 Conceptual Interfaces

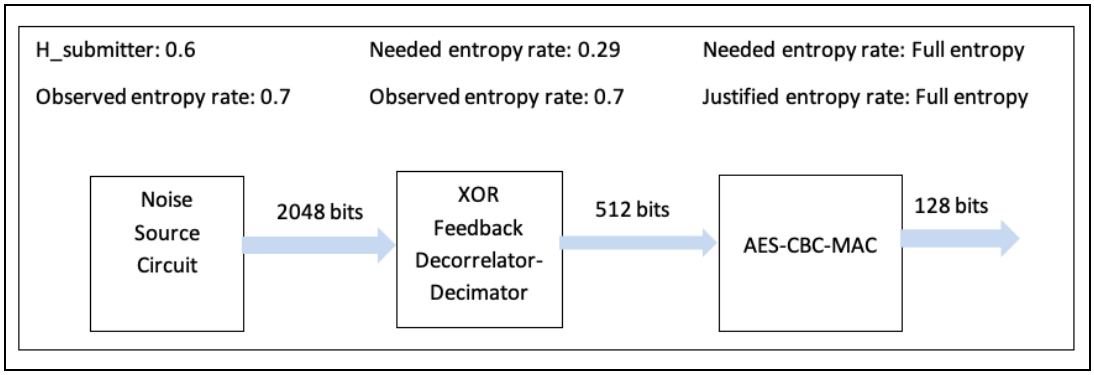
For consuming applications running in software on the CPU, `GetEntropy(n)` is implemented by the `RdSeed` instruction, where *n* can be one of 16, 32 or 64, depending on the size of the target register.

Internally to the security boundary, for feeding conditioner output data to the DRBG, `Get_entropy()` is implemented in digital logic between the conditioner and DRBG in the form of a 128-bit wide FIFO.

7 Min Entropy Rate

Figure 7-1 illustrates the required min-entropy rate and the actual observed min-entropy rate of the noise source and the chain of conditioners consisting of a non-vetted XOR Feedback Decorrelator-Decimator and a vetted AES-CBC-MAC. The XOR Feedback Decorrelator-Decimator is a digitizer per design, but for the sake of 90B compliance, it is treated as a non-vetted conditioner.

Figure 7-1. Entropy Levels on Noise Source and Conditioning Chain



The output of the AES-CBC-MAC conditioner has the full entropy, given that the input to the AES-CBC-MAC has an entropy rate that is greater than 0.29. The ≥0.29 entropy rate requirement from the digitized noise source is based on the SP 800-90B section 3.1.5.1.1 equation for the minimum input entropy requirement of the vetted AES-CBC-MAC conditioner.

The 0.6 entropy rate on the pre-digitizer data is a design target across all variants of silicon. The actual observed entropy rate on the noise source prior to digitization on the Intel CPU is greater than 70%. The digitization stage does not reduce the entropy rate, and it is observed that the entropy rate of the post-digitizer data feeding into the AES-CBC-MAC conditioner is greater than 0.7. The difference between the 0.29 and 0.7 entropy rates is the engineering margin in the design of the entropy source.

8 Health Tests

The DRNG includes:

- Continuous Health Tests (CHT).
- Startup Noise Source Health Tests.
- Startup Logic Integrity BIST.

The vendor defined Continuous Health Test is composed of a short-term test yielding a pass/fail over individual 256-bit blocks of noise source data and a long-term evaluation of the pass/fail history of the past 256 block (totaling 65536 bits) to infer an entropy source failure. The failure condition is invoked when the pass rate drops below 50%.

The logic integrity test is one of the startup tests. This performs a test of the digital logic by running deterministic random sequences through all the logic and testing the resulting output against the expected result.

The Startup Noise Source Health Test involves running the CHTs for a probationary period of 65536 bits from the noise source. When the test is complete, assuming the test passes, the RNG enters the operational state. This happens during startup and completes before the first instructions can execute. The startup test is invoked at power-on or exiting the reset state. So, the startup tests can be invoked by power cycling or resetting.

A failure in any of the startup tests (logic integrity or noise source health test) will be reflected as a BIST failure in the internal status register which leads to an MCHECK failure.

Following the startup tests, the CHTs continue to run. Should failure condition of the CHT test be encountered after the startup tests have completes, this may be either the result of a soft error or a hard error. The test will continue to run and should the entropy quality return, it will exit the failure state. In the failure state, no more random numbers are issued, and the failure state is reflected in the BIST status register result bits. Should some condition exist (for example, out of specification operating condition), cessation of that condition will lead to resumption of the supply of random numbers.

9 Maintenance

There are no maintenance action requirements.

10 Required Testing

No user or module integrator testing of the entropy source is required or available. The built in noise source continuous health tests and boot time hardware integrity tests verify the full functioning of the RNG.