Intel Digital Random Number Generator SP800-90B Non-Proprietary Public Use Document

Intel Entropy Source

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Intel Confidential

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Revision History

Revision Number	Description	Date
0.3.4	• Initial release	May 2023

1 Description

The Intel Digital Random Number Generator Entropy Source is a physical (P) entropy source.

The circuit component is RNG_ES_ICX_1.0

The synthesizable RTL component is ICX-COOP-RTL1.0

All components of the entropy source are hardware, consisting of logical and electronic components bounded in a rectangle of silicon. There is no firmware or software within the entropy source.

The entropic data from the entropy source is Non- Independent and Identically Distributed (IID).

This PUD is applicable to the following products:

Table 1-1. List of Applicable Devices

Processor Name	Processor Name
Intel® Xeon® Silver 4310 Processor	Intel® Xeon® Gold 5315Y Processor
Intel® Xeon® Silver 4314 Processor	Intel® Xeon® Gold 5318N Processor
Intel® Xeon® Silver 4316 Processor	Intel® Xeon® Gold 5318S Processor
Intel® Xeon® Gold 5317 Processor	Intel® Xeon® Gold 5318Y Processor
Intel® Xeon® Gold 5320 Processor	Intel® Xeon® Gold 5320T Processor
Intel® Xeon® Gold 6326 Processor	Intel® Xeon® Gold 6312U Processor
Intel® Xeon® Gold 6334 Processor	Intel® Xeon® Gold 6336Y Processor
Intel® Xeon® Gold 6342 Processor	Intel® Xeon® Gold 6338T Processor
Intel® Xeon® Silver 4309Y Processor	Intel® Xeon® W-3323 Processor
Intel® Xeon® Silver 4310T Processor	Intel® Xeon® W-3335 Processor

2 Security Boundary

The Digital Random Number Generator (DRNG)security boundary surrounds the set of components referred to as the DRNG core, that includes the noise source, digitizer, Continuous Health Tests (CHT), Advanced Encryption Standard (AES)- Cipher Block Chaining - Message Authentication Code (CBC-MAC) Vetted Conditioning Component, Deterministic Random Bit Generator (DRBG), Non-deterministic Random Bit Generator (NRBG) and register interface.

For use as a full entropy source, the NRBG output of the DRNG is the necessary output. This is accessed through the Intel CPU instruction “RdSeed”.

The security boundary is a sub boundary within the DRNG. Components outside the security boundary but within the DRNG are to attach to the local bus, clock and power systems on the chip.

The DRNG security boundary is not a Federal Information Processing Standard (FIPS) 140 security boundary. It is designed to be usable within a larger FIPS 140 security boundary through compliance to SP800-90Arev1, B and draft C along with relevant requirements in ISO/IEC 19790-2012 and FIPS 140-3.

The bold outline in Figure 2-1 shows the security boundary of the entropy source and other RNG components.

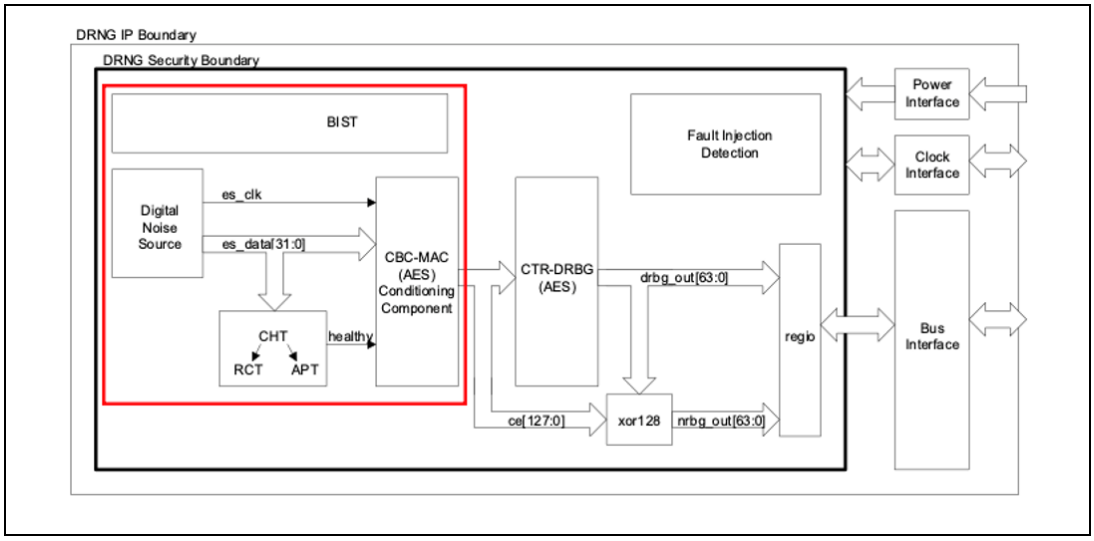
The NRBG output path to the region block is the output of the full entropy source, as an RBG3 construction.

The DRBG output path to the region block is the output of the DRBG, as an RBG2 construction.

The NRBG construction is the XOR (RBG3) construction NRBG from Draft SP800-90C. This XORs the output of the conditioner with an output from the DRBG to form the NRBG output. The strength of the XOR is entirely dependent on the full entropy of the conditioner output. The DRBG’s input into the XOR, as well as the XOR operation itself are not considered part of the conditioning chain.

The width of these operations is 128 bits, driven by the output size of AES. The registers sizes are 64 bits and in the logic, this width transforming is performed using a FIFO that is 64 bits wide and takes in 128 bits as two 64-bit entries and outputs 64 bits to match the register width.

Figure 2-1. DRBG Security Boundary



In the context of an Intel CPU, the DRNG register that presents the NRBG output to the local bus is called `egetdata`. This register is read by the CPU whenever the `RdSeed` instruction is executed. The result is passed to the target register of the instruction and the success or failure signaled in the carry flag.

This report is applicable to the devices in Table 1-1. The silicon manufacturing process, Integrated Circuit (IC) design and DRNG design is identical for each of these devices. Differences between these devices are the set of enabled features, which has no influence on the RNG behavior.

3 Operating Conditions

The entropy source is guaranteed to operate within the designated operating envelope in the data sheet of the chip. In **Intel® Xeon® Gold 5315Y Processor** the operating envelope is as follows:

Table 3-1. Operating Conditions

Parameter	Minimum	Maximum
Temperature	0 °C	81 °C

These conditions are taken from the Intel Automated Relational Knowledge-Base (ARK) specifications:

https://www.intel.com/content/www/us/en/products/sku/215286/intel-xeon-gold-5315y-processor-12m-cache-3-20-ghz/specifications.html

4 Configuration Settings

There are no configuration settings accessible at any privilege level to software running in the CPU.

5 Physical Security Mechanisms

The RNG contains a security boundary described in Section 2. In the operating mode of the RNG, there is hardware enforcement of the security of the boundary.

Specifically:

- Diagnostic output of raw data from the boundary is disabled.
- Debugging port access to internal state of the RNG is disabled at the boundary.
- Configuration input written to registers is ignored and the default configuration is enforced.
- Algorithms are implemented to detect stuck output failures.
- Register write privileges are enforced in hardware.

When an alarm is triggered, the RNG resets itself and re-runs Built-In Self-Test (BIST). It is not possible to distinguish between a failure due to attack or environmental bounds violation or a rare false positive error. The re-running of BIST will lead to the RNG failing if the BIST fails. In the case of a transitory error, the RNG will recover when BIST is re-run.

The packaging of the chip is a tamper evident enclosure.

6 Conceptual Interfaces

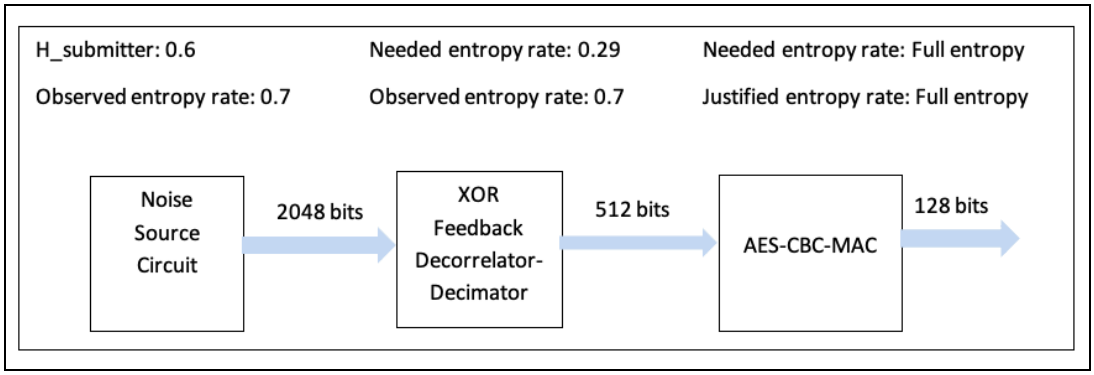
For consuming applications running in software on the CPU, `GetEntropy(n)` is implemented by the `RdSeed` instruction, where *n* can be one of 16, 32 or 64, depending on the size of the target register.

Internally to the security boundary, for feeding conditioner output data to the DRBG, `Get_entropy()` is implemented in digital logic between the conditioner and DRBG in the form of a 128-bit wide First In, First Out (FIFO).

7 Min Entropy Rate

Figure 7-1 illustrates the required min-entropy rate and the actual observed min-entropy rate of the noise source and the chain of conditioners consisting of a non-vetted XOR Feedback Decorrelator-Decimator and a vetted AES-CBC-MAC. The XOR Feedback Decorrelator-Decimator is a digitizer per design, but for the sake of 90B compliance, it is treated as a non-vetted conditioner.

Figure 7-1. Entropy Levels on Noise Source and Conditioning Chain



The output of the AES-CBC-MAC conditioner has the full entropy, given that the input to the AES-CBC-MAC has an entropy rate that is greater than 0.29. The ≥0.29 entropy rate requirement from the digitized noise source is based on the SP 800-90B section 3.1.5.1.1 equation for the minimum input entropy requirement of the vetted AES-CBC-MAC conditioner.

The 0.6 entropy rate on the pre-digitizer data is a design target across all variants of silicon. The actual observed entropy rate on the noise source prior to digitization on the Intel CPU is greater than 70%. The digitization stage does not reduce the entropy rate, and it is observed that the entropy rate of the post-digitizer data feeding into the AES-CBC-MAC conditioner is greater than 0.7. The difference between the 0.29 and 0.7 entropy rates is the engineering margin in the design of the entropy source.

8 Health Tests

The DRNG includes:

- Continuous Health Tests (CHT).
- Startup Noise Source Health Tests.
- Startup Logic Integrity BIST.

The vendor defined Continuous Health Test is composed of a short-term test yielding a pass/fail over individual 256-bit blocks of noise source data and a long-term evaluation of the pass/fail history of the past 256 block (totaling 65536 bits) to infer an entropy source failure. The failure condition is invoked when the pass rate drops below 50%.

The logic integrity test is one of the startup tests. This performs a test of the digital logic by running deterministic random sequences through all the logic and testing the resulting output against the expected result.

The Startup Noise Source Health Test involves running the CHTs for a probationary period of 65536 bits from the noise source. When the test is complete, assuming the test passes, the RNG enters the operational state. This happens during startup and completes before the first instructions can execute. The startup test is invoked at power-on or exiting the reset state. So, the startup tests can be invoked by power cycling or resetting.

A failure in any of the startup tests (logic integrity or noise source health test) will be reflected as a BIST failure in the internal status register which leads to an MCHECK failure.

Following the startup tests, the CHTs continue to run. Should failure condition of the CHT test be encountered after the startup tests have completes, this may be either the result of a soft error or a hard error. The test will continue to run and should the entropy quality return, it will exit the failure state. In the failure state, no more random numbers are issued, and the failure state is reflected in the BIST status register result bits. Should some condition exist (for example, out of specification operating condition), cessation of that condition will lead to resumption of the supply of random numbers.

9 Maintenance

There are no maintenance action requirements.

10 Required Testing

We performed raw noise testing using the non-IID lower bound entropy tests of the SP800-90B Entropy Assessment software tool, showing the entropy from the noise source to exceed the minimum input threshold of 0.299 of the vetted conditioning components.

We performed restart testing using the SP800-90B Entropy Assessment software tool, showing the startup min entropy of *Hr* and *Hc* to be greater than 50% of *HI*.